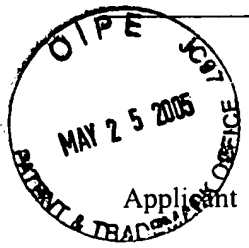
Docket No.: IMEC329.001AUS

Please Direct All Correspondence to Customer Number **20995**



TRANSMITTAL LETTER

INFORMATION DISCLOSURE STATEMENT

Applicant	:	Catthoor, et al.
App. No	:	10/817,310
Filed	:	April 2, 2004
For	:	DESIGN METHOD FOR ESSENTIALLY DIGITAL SYSTEMS AND COMPONENTS THEREOF AND ESSENTIALLY DIGITAL SYSTEMS MADE IN ACCORDANCE WITH THE METHOD
Examiner	:	DINH, PAUL
Art Unit	:	2825

CERTIFICATE OF MAILING

I hereby certify that this correspondence and all marked attachments are being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on

5/23/2005
(Date)

Eric M. Nelson, Reg. No. 43,829

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Enclosed for filing in the above-identified application are:

(X) An Information Disclosure Statement and PTO/SB/08 equivalent listing references for consideration:

- (X) Listing 6 references.
- (X) Enclosing 6 references.

(X) A copy of European Search Report.

(X) The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment, to Account No. 11-1410.

(X) Return prepaid postcard.

Eric M. Nelson
Registration No. 43,829
Attorney of Record
Customer No. 20,995
(619) 235-8550

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Docket No.: IMEC329.001AUS **Customer No. 20,995**

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(Date)

E. D. N.
Eric M. Nelson, Reg. No. 43,829

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Enclosed for filing in the above-identified application is an Information Disclosure Statement by Applicant (PTO/SB/08 equivalent) listing 6 references to be considered by the Examiner. Also enclosed are 6 foreign patent references and/or non-patent literature as listed on the Information Disclosure Statement. Also enclosed is a copy of European Search Report.

This Information Disclosure Statement is being filed before the receipt of a first Office Action on the merits, and no fee is required in accordance with 37 C.F.R. § 1.97(b)(3). Further, even if a first Office Action on the merits was mailed before the mailing date of this Statement, no fee is required as set forth below in 37 C.F.R. §§ 1.97(c) and 1.97(e)(1).

CERTIFICATION UNDER 37 C.F.R. § 1.97(e)(1)

I hereby certify that each item of information contained in this Statement was first cited in a communication from a foreign Patent Office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: 5/23/2005

By: _____

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PTO/SB/08 Equivalent

INFORMATION DISCLOSURE STATEMENT BY APPLICANT		
	Application No.	10/817,310
	Filing Date	April 2, 2004
	First Named Inventor	Cathoor et al.
	Art Unit	2825
(Multiple sheets used when necessary)	Examiner	Unassigned
SHEET 1 OF 1	Attorney Docket No.	IMEC329.001AUS

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number *Number - Kind Code (if known)* Example: 1,234,567 B1	Publication Date MM-DD-YYYY	Name of Patentee or Applicant	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Foreign Patent Document *Country Code-Number-Kind Code* Example: JP 1234567 A1	Publication Date MM-DD-YYYY	Name of Patentee or Applicant	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear	T[1]

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[1]
	1	BROCKMEYER E ET AL: "Systematic cycle budget versus system power trade-off: a new perspective on system exploration of real-time data-dominated applications" LOW POWER ELECTRONICS AND DESIGN, 2000. ISLPED '00. PROCEEDINGS OF THE 2000 INTERNATIONAL SYMPOSIUM ON JULY 26-27, 2000, PISCATAWAY, NJ, USA,IEEE, 26 July 2000 (2000-07-26), pages 137-142, XP010517318 ISBN: 1-58113-190-9	
	2	GIVARGIS T ET AL: "System-level exploration for Pareto-optimal configurations in parameterized systems-on-a-chip" IEEE/ACM INTERNATIONAL CONFERENCE ON COMPUTER AIDED DESIGN. ICCAD 2001. IEEE/ACM DIGEST OF TECHNICAL PAPERS (CAT. NO.O1CH37281) IEEE PISCATAWAY, NJ, USA, 8 November 2001 (2001-11-08), pages 25-30, XP002323201 ISBN: 0-7803-7247-6	
	3	GRUN P ET AL: "Memory system connectivity exploration" PROCEEDINGS 2002 DESIGN, AUTOMATION AND TEST IN EUROPE CONFERENCE AND EXHIBITION IEEE COMPUT. SOC LOS ALAMITOS, CA, USA, 4 March 2002 (2002-03-04), pages 894-901, XP002323202 ISBN: 0-7695-1471-5	
	4	PAPANIKOLAOU A ET AL: "Global Interconnect Trade-off For Technology Over Memory Modules To Application Level: Case Study" INT. WORKSHOP SYST. LEVEL INTERCONNECT PREDICT.; INTERNATIONAL WORKSHOP ON SYSTEM LEVEL INTERCONNECT PREDICTION 2003, 2003, pages 125-132, XP002323252	
	5	PAPANIKOLAOU A ET AL: "Interconnect Exploration for Future Wire Dominated Technologies" INT. WORKSHOP SYST. LEVEL INTERCONNECT PREDICT.; INTERNATIONAL WORKSHOP ON SYSTEM LEVEL INTERCONNECT PREDICTION 2002, 2002, pages 105-106, XP002323203	
	6	YUNSI FEI ET AL: "Functional partitioning for low power distributed systems of systems-on-a-chip" DESIGN AUTOMATION CONFERENCE, 2002. PROCEEDINGS OF ASP-DAC 2002. 7TH ASIA AND SOUTH PACIFIC AND THE 15TH INTERNATIONAL CONFERENCE ON VLSI DESIGN. PROCEEDINGS. BANGALORE, INDIA 7-11 JAN. 2002, LOS ALAMITOS, CA, USA,IEEE COMPUT. SOC, US, 7 January 2002 {2002-01-07), pages 274-281, XP010588114 ISBN: 0-7695-1441-3	

1713293 bts 051605

Examiner Signature	Date Considered

***Examiner:** Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

T[1] - Place a check mark in this area when an English language Translation is attached.